1-7.

8. (previously presented) The semiconductor circuit of Claim 10,

wherein the substrate comprises a package type selected from the group consisting of a ball grid array, a pin grid array, and a column grid array.

9. (previously presented) The semiconductor circuit of Claim 10,

wherein the substrate further comprises a plurality of recessed holes, each hole adapted to accept one of the first plurality of bumps.

10. (currently amended) A semiconductor circuit comprising:

a semiconductor die comprising a first plurality of electrical contacts and a second plurality of electrical contacts;

a first plurality of conductive bumps wherein at least one bump in the first plurality is conductively connected to at least one of the first plurality of electrical contacts;

a second plurality of conductive bumps, wherein at least one bump in the second plurality is conductively connected to at least one of the second plurality of electrical contacts; [[and]]

wherein the average size of the first plurality of conductive bumps is ~~at least 20%~~ larger than the average size of the second plurality of conductive bumps[[.]];

a substrate having a plurality of electrical contacts coupled to the first plurality of conductive bumps and the second plurality of conductive bumps; and

a built up layer between the substrate and the second plurality of bumps wherein the first plurality of bumps are substantially coplanar with the second plurality of bumps relative to the semiconductor die.

11. (original) The semiconductor circuit of Claim 10,

wherein the average size of the first plurality of conductive bumps is at least 100% larger than the average size of the second plurality of bumps.

12. (previously amended) The semiconductor circuit of Claim 10,

wherein the average size of the first plurality of conductive bumps is at least 200% larger than the average size of the second plurality of bumps.

13. (canceled)

14. (currently amended) A semiconductor circuit comprising:

a semiconductor die comprising a first plurality of electrical contacts and a second plurality of electrical contacts;

a first plurality of conductive bumps wherein at least one bump in the first plurality is conductively connected to at least one of the first plurality of electrical contacts;

a second plurality of conductive bumps, wherein at least one bump in the second plurality is conductively connected to at least one of the second plurality of electrical contacts;

wherein the average size of the first plurality of conductive bumps is at least 20% larger than the average size of the second plurality of conductive bumps;

a substrate having a plurality of electrical contacts coupled to the first plurality of conductive bumps and the second plurality of conductive bumps; and

a built up layer between the die and the second plurality of bumps; and wherein the first plurality of bumps are substantially coplanar with the second plurality of bumps with respect to their surfaces opposite the surface of the die.

15. (current amended) A method of making a semiconductor circuit, comprising:

providing a semiconductor die comprising a first plurality of electrical contacts and a second plurality of electrical contacts;

conductively connecting to the die a first plurality of conductive bumps wherein at least one bump in the first plurality is conductively connected to at least one of the first plurality of electrical contacts;

conductively connecting to the die a second plurality of conductive bumps, wherein at least one bump in the second plurality is conductively connected to at least one of the second plurality of electrical contacts; [[and]] wherein the average size of the first plurality of conductive bumps is at least 20% larger than the average size of the second plurality of conductive bumps [[.]];

providing a substrate having a plurality of electrical contacts and coupling the electrical contacts to the first plurality of conductive bumps and the second plurality of conductive bumps; and

forming a built-up layer between the substrate and the second plurality of bumps such that the first plurality of bumps are substantially coplanar with the second plurality of bumps relative to the semiconductor die.

16-20. (canceled)